WHAT IS CLAIMED IS:

1. A microcomputer comprising:

(a) a cache;

(b) a central processing unit, said cache and said central processing unit both being fabricated in one chip; and

(c) a memory storing commands to be executed by said central processing unit, said memory storing interruption handling routine therein.

2. The microcomputer as set forth in claim 1, wherein a program is written into said memory by switching memory maps when said microcomputer is turned on.

3. The microcomputer as set forth in claim 1, wherein said memory is comprised of a random access memory (RAM).

4. A microcomputer comprising:

(a) a central processing unit;

(b) a bus controller electrically connected to said central processing unit through a first bus;

(c) a command cache electrically connected to said central processing unit through a second bus, and to said bus controller through a third bus; and

(d) a command memory electrically connected to said second bus through a fourth bus, and storing interruption handling routine therein.

5. The microcomputer as set forth in claim 4, further comprising a memory controller electrically connected to said bus controller through a fifth bus, to said command memory through a sixth bus, and to an external memory through a seventh bus.

6. The microcomputer as set forth in claim 5, wherein said central processing unit, if said command cache stores a command to be executed by said central processing unit, reads said command out of said command cache, and executes the thus read-out command, and if said command cache does not store a command to be executed by said central processing unit, reads a command out of said external memory, and executes the thus read-out command.

7. The microcomputer as set forth in claim 4, wherein said central processing unit reads a command out of said command memory, and executes said interruption handling routine, when interruption occurs.

8. The microcomputer as set forth in claim 4, further comprising an external terminal electrically connected to said central processing unit, and wherein a region in which said command memory is to be arranged is designated through said external terminal.

9. The microcomputer as set forth in claim 8, wherein said external terminal can be operated even while said central processing unit is in operation.

10. The microcomputer as set forth in claim 4, further comprising an external terminal electrically connected to said central processing unit, and wherein memory maps are switched through said external terminal.

11. The microcomputer as set forth in claim 4, further comprising an internal register, and wherein memory maps are switched by said internal register.

12. The microcomputer as set forth in claim 4, wherein said memory is comprised of a random access memory (RAM).